Appl. No. 08/883,118
Amdt. dated March 10, 2005
Reply to Office action of September 14, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A bus system, comprising:

~~(a)~~ a plurality of bus elements, with each of the plurality of bus elements making requests for access to at least one other bus element;

~~(b)~~ a central unit having a plurality of bus input ports and a plurality of bus outputs, with the central unit selectively coupling at least one of the inputs to at least one of the outputs, the central unit providing for an arbitrated, point-to-point coupling of a particular one of the plurality of bus elements with the at least one other bus element;

~~(c)~~ a first plurality of uni-directional point-to-point buses ("first buses") for coupling in a first direction the bus elements to the central unit bus inputs;

~~(d)~~ a second plurality of uni-directional point-to-point buses ("second buses") for coupling in a second direction each output of the central unit to a respective bus element; and

~~(e)~~ arbitration logic connected to the plurality of bus inputs of the central unit to which the first plurality of unidirectional point-to-point buses connect, the arbitration logic for granting each of the bus elements access to the at least one other bus element through the central unit one at a time based upon the requests from the bus elements;

wherein each bus input port comprises an input state device, a buffer coupled to the input state device, a port multiplexer coupled to the buffer and the input state device, and validity logic that couples to the state device and that receives a control signal from the arbitration logic, said arbitration logic grants the input port access to the bus system and the validity logic provides an output to the port multiplexer.

2. (Previously presented) A system as recited in claim 1, wherein the system further includes a first state device that is disposed at the output of the central unit, the state device for controlling the output of the central unit.

3. (Canceled).

4. (Canceled).

5. (Canceled).

6. (Currently amended) A system as recited in claim ~~5~~1, wherein the arbitration logic is part of the central unit.

7. (Currently amended) A system as recited in claim ~~6~~1, wherein the arbitration logic includes a scheduler and an arbiter, with the scheduler and arbiter being connected.

8. (Original) A system as recited in claim 1, wherein the bus elements include a plurality of central processing units and a shared memory.

9. (Original) A system as recited in claim 8, wherein the shared memory further comprises a plurality of memory modules with a single one of the first buses and a single one of the second buses being provided for coupling to the memory.

10. (Canceled).

11. (Canceled).

12. (Canceled).

13. (Canceled).

14. (Canceled).

15. (Currently amended) A system as recited in claim ~~14~~8, ~~wherein the multiplexer circuitry, comprises~~further comprising:

a first multiplexer which has as inputs a first bus from each of the central processing units and providing an output coupled to the second bus from the central unit to the shared memory; and

a second multiplexer which has as a first input the output of the first multiplexer and as a second input the first bus from the shared memory to the central unit, with the output of the second multiplexer being connected to each of the second buses leading to the central processing units.

16. (Original) A system as recited in claim 15, wherein the system further includes a first state device at the output of the second multiplexer, with the output of the first state device being connected to the second buses leading to the central processing units.

17. (Original) A system as recited in claim 16, wherein the system further includes at least one driver between the output of the first state device and the second buses leading to the central processing units.

18. (Original) A system as recited in claim 17, wherein the central unit further includes a memory controller, with the memory controller providing at its output the second bus to the memory and having as an input the first bus from the memory, with the memory controller connecting the first bus to the second multiplexer and connecting the output of the first multiplexer to the second bus.

19. (Previously presented) The system as recited in claim 18, wherein the system further includes port select logic that connects each of the first buses from the plurality of central processing units to the first multiplexer.

20. (Canceled).

21. (Currently amended) The system as recited in claim ~~20~~19, wherein the arbitration logic includes an arbitrator coupled to the validity logic, and scheduling logic coupled to the port multiplexer and the arbitrator.

22. (Currently amended) The system as recited in claim 21, wherein ~~the~~ outputs of the port multiplexers ~~in the port logic for each of the central processing units is~~ are connected to the inputs of the first multiplexer, with the port select logic comprising logic responsive to the outputs of the port multiplexers and to an input from the arbitrator to control the first multiplexer ~~such as to selectively couple one of its inputs to its output~~.

23. (Currently amended) The system as recited in claim ~~22~~21, wherein the scheduling logic includes logic to grant the input ports access on a round robin basis.

24. (Currently amended) A system as recited in claim 23, wherein the port select logic comprises:

a barrel shifter;

a first priority encoder having as inputs the outputs of the barrel shifter;

a schedule port ID multiplexer having as a first input the output of the priority decoder;

left shift one logic having a input coupled to the output of the first priority encoder and providing an output which is left shifted by one;

a next port multiplexer having as a first input the output of the left shift one logic;

a second state device coupled to the output of the next port multiplexer, the output of the second state device coupled back as a second input to next port multiplexer and as an input to the barrel shifter;

a third state device at the output of the schedule port ID multiplexer providing its output as a second input to the schedule port ID multiplexer, the output of the schedule port ID multiplexer also coupled to control the first multiplexer; and

port select logic for controlling the schedule port ID multiplexer to switch between the input of the priority encoder and the fed back input from the third state device.

25. (Previously presented) The system as recited in claim 24, wherein each of the first buses includes at least one function code (FC) line indicative of the beginning and end of a transmission on the bus and the port select logic is responsive to the at least one function code (FC) line to switch the schedule port ID multiplexer to the next port.

26. (Original) The system as recited in claim 25, wherein the port select logic includes an old FC multiplexer having as inputs the FC lines from each of the ports, with the FC multiplexer being controlled by the output of the third state device; and

a port select generator having as one input the output of the old FC multiplexer and as a second input a scheduler grant input from the arbitrator.

27. (Previously presented) The system as recited in claim 24, wherein at least some of the central processing units include cache memory with each of the first buses including a "snoopy hit line" indicating that the addresses in a read command issued by another central processing unit are contained within its cache memory, with the port select logic further comprising:

a second priority encoder having as inputs the "snoopy hit lines" from the buses;

an OR gate having as inputs said "snoopy hit lines", the output of the OR gate providing an input to the port select generator; and

the port select generator having as a further input a "snoopy hit shadow signal" indicating the period during which "snoopy hit signals" may occur, the output of the second priority encoder designating a "snoopy port" at which a "snoopy hit" has occurred and being coupled as a third input to the schedule port ID multiplexer, the port select generator, in response to receiving to the "snoopy hit signal" within the period of the "snoopy hit shadow" selects as the port to which access is to be granted, the "snoopy port" designated at the output of the priority encoder.

28. (Original) The system as recited in claim 27, wherein the central unit further includes at least one resource status unit including a memory map status unit indicating the status of modules in the shared memory, with the arbitrator including a resource check logic having as inputs the outputs from the resource status units, the output of the first multiplexer and the output of the memory controller, the resource checker responsive thereto to provide outputs to the port logic and to the port select logic in the schedule logic and also to provide an output to the second multiplexer to select between resources, the resources including data from one of the central processing units at the output of the first multiplexer and memory data from the shared memory modules.

29. (Original) The system as recited in claim 28, wherein the resource check logic includes a command decoder receiving as an input the output from the first multiplexer; and

a command and resource check module having as one input the output of the command decoder and as additional inputs the outputs of the units indicating the status of modules of the shared memory; and

a timing circuit for generating the "snoopy hit shadow".

30. (Canceled).

31. (Canceled).

32. (Canceled).

33. (Currently amended) A method of implementing a high speed bus to which a plurality of bus elements are coupled comprising ~~the steps of~~:

~~(a)~~ coupling with a first uni-directional bus in a first direction each of the bus elements to a central unit via one of a plurality of first bus inputs;

~~(b)~~ selecting ~~with arbitration means~~ one of the first bus inputs to the central unit for output to at least one of a plurality of central unit outputs; ~~and~~

~~(c)~~ coupling, with a second uni-directional bus in a second direction, each of the plurality of central unit outputs to a respective one of the plurality of bus elements; ~~and~~

~~(d)~~ providing for an arbitrated, point-to-point coupling of a particular one of the plurality of bus elements with at least another bus element;

receiving commands, each command followed by an address and/or data and/or additional commands;

storing up to three words output by a bus element at the central unit;

arbitrating access to the bus at the output of the central unit, including granting access to one of the bus element inputs by providing a stored command to the output and on successive cycles providing additional words stored at the central unit on the output; and

when all stored words have been provided on the output on the next and subsequent cycles providing any input words from the bus ele4ment directly on the output whereby, by storing a number of words in the central unit, once the bus element is granted access to the bus, a continual flow of data will occur without any dead time.

34. (Original) The method as recited in claim 33, wherein the bus elements include a plurality of central processing units and a shared memory.

35. (Currently amended) The method as recited in claim 34, wherein ~~the~~ selecting ~~step~~ further comprises selecting between the inputs on the first buses from the central processing units and the second bus from the shared memory.

36. (Canceled).

37. (Previously presented) The bus system as recited in claim 2, wherein the first state device includes a latch.

38. (Currently amended) The bus system as recited in claim ~~5~~1, wherein ~~the~~ each ~~of the second~~ input state devices ~~include~~ comprises a latch.

39. (Previously presented) The bus system as recited in claim 1, wherein a bus element includes a CPU.

40. (Canceled).